Faiyaj Rahman

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Education

University of Michigan — Ann Arbor, MI
B.S.E. in Computer Engineering — *May 2028*
- **Relevant Coursework:** Data Structures and Algorithms, Computer Organization, Object Oriented Programming, Discrete Math, Computing Systems, Computational Linear Algebra, Vector Calculus

Honors & Awards

Jane Street FOCUS Participant — May 2026
*Competitive quantitative trading and software engineering program, selected from **1000+** applicants* — *New York, NY*

Work Experience

Software Engineering Intern — May 2026 – Present
Bosch | Agentic AI, Python, AWS, RESTAPI, CI/CD, Docker, Kubernetes, Bash, Git — *Farmington Hills, MI*
- Architecting a modular platform hosting all organization file-conversion tools, first shipping CAN `.asc` to `MF4` with DBC channel mapping for MDA; drops the licensed CANalyzer dependency, saving **20+** engineer-hours monthly.
- Prototyping org-wide agentic AI by wiring LLM agents to internal CLIs and Git, cutting development time by **30%**.
- Deployed a fleet monitoring platform to AWS and scripted multi-tenant vehicle analytics scaling to **5000+** vehicles.
- Engineered a multi-threaded GUI used by **100+** developers to build Python executables, saving **15K** dollars costs.

Co-Founder & Software Developer — Nov. 2025 – Present
Saf | Darul Uloom Michigan | Claude, TypeScript, React, Supabase, PostgreSQL, Tailwind, Git — *Warren, MI*
- Co-founded Saf under Darul Uloom Michigan, a platform unifying **5** products for the Muslim community: Arshad (school management), Tajul Haramain (Pilgramage packages), school admissions, prayer times, and staff time clock.
- Moved password/role verification server-side into a Supabase edge function, enforcing Postgres RLS across **4** portals.
- Shipped **300+** PRs and **43** deploys with typed CI and forward-only SQL migrations for **30+** educators and admins.
- Integrating AI and an investor demo hub with **200+** users ahead of a venture raise and scholar-backed public launch.

Software Engineer — Aug. 2025 – Present
MRacing FSAE | Cursor, C/C++, Embedded Systems/Software, Linux, CAN, Raspberry Pi, Gitlab — *Ann Arbor, MI*
- Built a C++ Raspberry Pi dashboard decoding **1000+** CAN messages/sec into signals and fault states across **3** pages.
- Refactored the legacy Python GUI codebase into C++, cutting latency ∼**100**× and improving signal timing ∼**50%**.
- Collaborated with engineers in testing to debug/validate software, ensuring ∼**100%** data consistency across signals.

Undergraduate Research Software Developer — Sep. 2025 – May 2026
University of Michigan Electrical Vehicle Center | Claude, Python, Raspberry Pi, Figma, Simulink — *Ann Arbor, MI*
- Developed open-source Python software for an EV charging module, contributing to **$10k** in net savings for an OEM.
- Designed a Simulink FSM for system-safety logic and charging protocols, porting it to Python for pipeline integration.

Projects

Overround | *C++, Python, PyTorch, React, D3.js, FastAPI, PostgreSQL* — Jul. 2026 – Present
- Building a transformer with learned club embeddings over **18,000+** matches across five domestic leagues, solving cross-league calibration to predict UEFA Champions League outcomes, outperforming Dixon-Coles and Elo baselines.
- Engineering a multithreaded C++ Monte Carlo engine simulating the **36**-team league phase at **5,000+** sims per sec.

Limit Order Book & Matching Engine | *Claude, C++, Linux, Git* — May 2026 – Present
- Built a high-performance C++ limit order book with price–time priority, handling **10K–100K+** orders/sec for market orders, cancellations, modifications, and partial fills, achieving **sub-millisecond** execution for every core operations.
- Optimized execution using cache-efficient data structures, custom allocators, and tight memory layouts, reducing latency by ∼**40–60%** and validating throughput against **1M+** simulated order events under live-market conditions.

Low-Level Modulator | *Verilog, Assembly, FPGA, Digital Logic* — Jan. 2026 – Apr. 2026
- Engineered a **18**-instruction processor in Verilog on a DE2-115 FPGA driving a synthesizer with **40** assembly modules.
- Designed an integer-math DSP pipeline synthesizing **32-bit** audio from **3** wavetables with **5** modulations at **30 FPS**.

Technical Skills

Languages: C/C++, Python, JavaScript, TypeScript, Assembly, Java, SQL, Verilog, OCaml, MATLAB
Tools/Frameworks: Claude, Cursor, Codex, React, PostgreSQL, Linux, Git, Node, STM32, Raspberry Pi, Altium, CAD